Section 102 Rejections:

Claims 1-3, 8, and 10-11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,314,575 to Yanagida. (hereinafter "Yanagida"). Claims 1-4, 7-8, 10-12, and 15 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,080,661 to Bothra. (hereinafter "Bothra"). As will be set forth in more detail below, the § 102 rejections of claims 1-4, 7-8, 10-12 and 15 are respectfully traversed.

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP § 2131. The cited art does not disclose all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

The cited art does not disclose etching a first portion of a dielectric layer with a first etch chemistry, which is selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride. Amended independent claim 1 recites in part: "[a] method for forming a semiconductor device, comprising: etching a first portion of a dielectric layer formed on a semiconductor topography with a first etch chemistry...etching a second portion of the dielectric layer with a second etch chemistry different from the first etch chemistry, wherein the first and second etch chemistries are selective to silicon nitride." Support for the amendments to the claim may be found in the Specification, for example, on page 27, lines 20-23 and page 30, lines 14-18.

Yanagida discloses a reactive ion etching method in which a silicon compound film is etched through a mask by a two-stage procedure. Yanagida, however, does not disclose etching a first portion of a dielectric layer with a first etch chemistry, which is selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride. For example, Yanagida states that "the silicon compound film to be etched in the method of the invention is a film made of various silicon compounds such as oxides, nitride and the like." (Yanagida -- col. 3, lines 33-35.) Yanagida also states that "according to the method of the invention, a silicon compound film formed on a suitable support can be etched to a desired depth at a high rate by etching it with a gas mainly composed of a hydrogen-free carbon fluoride." (Yanagida -- col. 2,

lines 64-68.) In addition, Yanagida states that "a silicon compound film such as SiO_2 film or SiN film is dry etched in a pattern by a two-stage procedure wherein high speed anisotropic etching is first affected using a gas mainly composed of a H-free carbon fluoride gas such as C_3F_8." (Yanagida -- col. 6, lines 34-38.) In this manner, Yanagida teaches etching a first portion of a dielectric layer with an etch chemistry that etches silicon nitride at a high speed. Therefore, such an etch chemistry is not selective to silicon nitride. As such, Yanagida does not teach or suggest etching a first portion of a dielectric layer with a first etch chemistry, which is selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride, as recited in claim 1. Consequently, Yanagida does not teach or suggest all limitations of claim 1.

Bothra discloses methods for fabricating gate and diffusion contacts in self-aligned contact processes. Bothra, however, does not disclose etching a first portion of a dielectric layer with a first etch chemistry, which is selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride. For example, Bothra states that "a silicon nitride etch will be performed to remove the exposed silicon nitride material 218 within the windows 220." (Bothra -- col. 7, lines 21-23.) Bothra also states that "in this preferred embodiment, the etching through the silicon nitride layer 218 will preferably be performed using the etching chemistries and conditions illustrated in table A below." (Bothra -- col. 7, lines 25-29.) The etch chemistry illustrated in this table is one of two etch chemistries disclosed by Bothra. In addition, Bothra states:

> Due to experimentally determined etch rate selectivities, the etching chemistries used to etch through the silicon nitride material 218 will only etch through the dielectric layer 216 at about one-third the rate of silicon nitride. As a result, when about 750 angstroms of the silicon nitride layer 218 is etched, a subsequent 100 percent overetch will only etch about 250 angstroms of dielectric material 216 (i.e., 750/3=250). (Bothra -- col. 7, line 54 - col. 8, line 2.)

In this manner, one of the two etch chemistries disclosed by Bothra is not selective to silicon nitride. Therefore, Bothra does not teach or suggest etching a first portion of a dielectric layer with a first etch chemistry, which is selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride, as recited in claim 1. As such, Bothra does not teach or suggest all limitations of claim 1.

For at least the aforementioned reasons, claim 1, as well as claims dependent therefrom, are not anticipated by the cited art. Accordingly, removal of the § 102 rejections of claims 1-4, 7-8, 10-12 and 15 is respectfully requested.

Section 103 Rejections:

Claims 1-5, 7-8, 10-22, and 24-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,337,285 to Ko (hereinafter "Ko '285") in view of Yanagida. Claims 9 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ko '285 in view of Yanagida and in further view of U.S. Patent No. 6,117,791 to Ko et al. (hereinafter "Ko '791). Claims 1-5 and 7-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,025,255 to Chen et al. (hereinafter "Chen") in view of Yanagida. Claims 4-5, 7, 9, and 12-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yanagida or Bothra. As set forth in more detail below, the rejections of claims 1-5 and 7-27 are respectfully traversed.

To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond,* 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984), MPEP 2143.01. The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

None of the cited art teaches or suggests etching a first portion of a dielectric layer with a first etch chemistry, which is substantially free of hydrogen and selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride, as recited in claim 1. As set forth in more detail above, Yanagida and Bothra do not teach or suggest all limitations of claim 1.

There is also no suggestion or motivation to modify the process of Yanagida such that Yanagida teaches all limitations of claim 1. For example, Yanagida states that "it is accordingly an object of the invention to provide an etching method wherein etching is performed at high rate with a reduced degree of damage on an underlying layer or layers." (Yanagida -- col. 2, lines 3-6.) As set forth in more detail above, Yanagida teaches etching a dielectric layer such as silicon nitride at a high rate. Therefore, modifying the process of Yanagida such that etching is performed with an etch chemistry that is selective to silicon nitride would prevent etching from being performed at a high rate thereby rendering the prior art invention of Yanagida being modified unsatisfactory for its intended purpose.

In addition, there is no suggestion or motivation to modify the process of Bothra such that Bothra teaches all limitations of claim 1. For example, Bothra states that "an invention for improved methods of fabricating conductive contacts down to diffusion regions and transistor gates in self-aligned contact processes is disclosed." (Bothra -- col. 5, lines 54-56.) Bothra discloses that the contacts are formed by etching through silicon nitride layer 218 and silicon nitride layer 214, as shown in Fig. 10 of Bothra. Therefore, modifying the process of Bothra such that etching is performed with an etch chemistry that is selective to silicon nitride would hinder etching through the silicon nitride layers, and may even prevent formation of the conductive contacts, thereby rendering the prior art invention of Bothra being modified unsatisfactory for its intended purpose.

Ko '285 discloses a two-step dual-chemistry process for etching through a selected portion of an insulating oxide layer. Ko '285, however, does not disclose etching a first portion of a dielectric layer with a first etch chemistry, which is substantially free of hydrogen and selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride. For example, as stated in the Office Action, "Ko fails to teach that said first etch chemistry is substantially free of hydrogen." (Office Action -- page 5.) The Office Action also states that "it would have been obvious for those skilled in the art to combine the teaching of Yanagida to the process of Ko to use the first etch chemistry substantially free of hydrogen as being claimed." (Office Action -- page 5.)

There is, however, no motivation to modify Ko '285 as suggested in the Office Action. For example, Ko '285 states that "a first C_xF_y (x>1)-type chemistry is used to etch the doped insulating oxide layer 24, with very good selectivity to the silicon nitride cap 22 and spacer 32 of the gate stacks 30." (Ko '285 -- col. 5, lines 65 - col. 6, line 1.) As set forth in more detail above, Yanagida, however, discloses

that the first etch chemistry of Yanagida etches silicon nitride at a very high rate. Therefore, neither Yanagida nor Ko '285 provide any motivation for combining the teaching of Yanagida and the process of Ko '285. As such, Ko '285 and Yanagida, either individually or in combination, do not teach, suggest, or provide motivation for etching a first portion of a dielectric layer with a first etch chemistry, which is substantially free of hydrogen and selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride, as recited in claim 1. Consequently, Ko '285 and Yanagida, either individually or in combination, do not teach or suggest all limitations of claim 1.

Ko '791 discloses an etchant with selectivity for doped silicon dioxide over undoped silicon dioxide and silicon nitride. Ko '791, however, does not disclose etching a first portion of a dielectric layer with a first etch chemistry, which is substantially free of hydrogen and selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride. For example, Ko '791 states that "turning now to FIG. 3, an etch step is depicted, wherein an etchant 30, which is introduced into an etch chamber (not shown) either with or without a carrier gas, attacks the areas of passivation layer 24 that are exposed through openings 28 of mask 26." (Ko '791 -- col. 7, lines 24-28.) Ko '791 also states that "etchant 30, which comprises a $C_2H_xF_y$-containing etchant of the present invention, etches an aperture through passivation layer 24." (Ko '791 -- col. 7, lines 36-38.) As such, Ko '285, Yanagida and Ko '791, either individually or in combination, do not teach, suggest, or provide motivation for etching a first portion of a dielectric layer with a first etch chemistry, which is substantially free of hydrogen and selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride, as recited in claim 1. Consequently, Ko '285, Yanagida and Ko '791, either individually or in combination, do not teach or suggest all limitations of claim 1.

Chen discloses a two step etching process for forming self-aligned contact. Chen, however, does not disclose etching a first portion of a dielectric layer with a first etch chemistry, which is substantially free of hydrogen and selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride. For example, as stated in the Office Action, "Chen et al fails to teach that said first etch chemistry is substantially free of hydrogen." (Office Action -- page 8.) The Office Action also states that "it would have been obvious for those skilled in the art to combine the teaching of Yanagida to the process of Chen et al to use the first etch chemistry substantially free of hydrogen as being claimed." (Office Action -- page 8.)

There is, however, no motivation to modify Chen as suggested in the Office Action. For example, Chen states that "these objects are accomplished by...controlling the rate of polymer formation. The procedure provides a first period during which a high etch rate selectivity of oxide to nitride is achieved by condition which cause heavy formation of polymer." (Chen -- col. 3, lines 60-65.) In addition, Chen states that "under these conditions vertical sidewalls are achieved and the oxide/nitride etch rates are in a ratio of about 20:1." (Chen -- col. 5, lines 56-58.) Furthermore, Chen states that "oxide/nitride etch rate selectivity . . . is raised by the addition of CH_2F_2. The increase in selectivity is attributed to polymer deposition over the nitride. The selection of the additive gas such as CH_2F_2 is made according to a rule where the number of hydrogen atoms must be equal to or greater than the number of fluorine atoms." (Chen -- col. 2, lines 61-65.) As set forth in more detail above, Yanagida, however, discloses that the first etch chemistry of Yanagida etches silicon nitride at a very high rate. Therefore, neither Yanagida nor Chen provide any motivation for combining the teaching of Yanagida and the process of Chen. As such, Chen and Yanagida, either individually or in combination, do not teach, suggest, or provide motivation for etching a first portion of a dielectric layer with a first etch chemistry, which is substantially free of hydrogen and selective to silicon nitride, and etching a second portion of the dielectric layer with a second etch chemistry, which is different than the first etch chemistry and selective to silicon nitride, as recited in claim 1. Consequently, Chen and Yanagida, either individually or in combination, do not teach or suggest all limitations of claim 1.

The cited art does not disclose etching a first portion of a dielectric layer with a first etch chemistry that is substantially free of hydrogen and etching a second portion of the dielectric layer, which has a thickness greater than about one half a height of gate structures, with a second etch chemistry. Independent claim 17 recites in part:

> . . . etching a first portion of the dielectric layer with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen; and etching a second portion of the dielectric layer with a second etch chemistry, wherein a thickness of the second portion of the dielectric layer is greater than approximately one half a height of the first and second gate structures.

For at least the reasons set forth above, the cited art does not teach or suggest etching a first portion of a dielectric layer with a first etch chemistry that is substantially free of hydrogen and etching a second portion of the dielectric layer, which has a thickness greater than about one half a height of gate structures, with a second etch chemistry, as recited in claim 17. For example, there is no motivation to combine the teachings of Yanagida with the process of either Ko '285 or Chen. In addition, if the

teachings of Yanagida are combined with the process or either Ko '285 or Chen, the modifications would render the invention of Ko '285 or Chen unsatisfactory for its intended purpose. For example, if Ko '285 is combined with Yanagida as suggested in the Office Action, Ko '285 and Yanagida teach that the process of Yanagida will cause the silicon nitride cap and spacer of the gate stacks of Ko '285 to be etched. In this manner, the etched silicon nitride cap and spacer of Ko '285 will erode thereby causing contact between the gate stacks and a contact structure formed in the etched portion of the dielectric layer. Similarly, Chen states that "under conditions of inadequate etch rate selectivities the nitride sidewalls 27 and top nitride cap layer 24 etch at rates whereby the insulative spacing provided by these elements is reduced by erosion of the nitride, resulting in subsequent shorts between bitline and wordline." (Chen -- col. 2, lines 22-26.) Therefore, if Chen is combined with Yanagida as suggested in the Office Action, Chen and Yanagida teach that the process of Yanagida will cause the nitride sidewalls and the top nitride cap of Chen to be eroded thereby causing shorts between bitlines and wordlines. Consequently, such modifications will render the processes of Ko '285 and Chen unsuitable for fabricating semiconductor devices. As such, none of the cited art, either individually or in combination, teaches or suggests all limitations of claim 17.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). MPEP 2143.01.

Even if the cited art can be modified, as suggested by the Office Action, the resultant modifications are not obvious because the prior art does not suggest the desirability of the modifications. None of the cited art, alone or in combination, suggests the desirability of the modifications proposed in the Office Action. As such, the modifications proposed by the Office Action are not obvious.

The cited art does not disclose etching a first portion of a substantially continuous dielectric layer adjacent to a gate structure with a first etch chemistry substantially free of hydrogen sufficiently to expose a sidewall spacer of the gate structure and etching a second portion of the dielectric layer with a second etch chemistry including a hydrofluorocarbon etchant sufficiently to expose a substrate under the dielectric layer. Independent claim 21 recites in part:

> . . . etching a first portion of a substantially continuous dielectric layer adjacent to a gate structure with a first etch chemistry substantially free of hydrogen sufficiently to expose a sidewall surface of said gate structure; and etching a second portion of the substantially continuous dielectric layer with a second etch chemistry comprising a hydrofluorocarbon etchant sufficiently to expose a substrate under said substantially continuous dielectric layer.

For at least the reasons set forth above, the cited art does not teach or suggest etching a first portion of a substantially continuous dielectric layer adjacent to a gate structure with a first etch chemistry substantially free of hydrogen sufficiently to expose a sidewall spacer of the gate structure and etching a second portion of the dielectric layer with a second etch chemistry including a hydrofluorocarbon etchant sufficiently to expose a substrate under the dielectric layer, as recited in claim 21. In addition, as set forth in more detail above, modifying the cited art as suggested in the Office Action would render the inventions unsuitable for their intended purpose. Therefore, there can be no motivation to modify the cited art as suggested in the Office Action. As such, none of the cited art, either individually or in combination, teaches or suggests all limitations of claim 21.

The Office Action states that "CO is an well-known etchant which has been used to improve etching profile while etching a dielectric layer." (Office Action -- page 9.) Applicants respectfully traverse this assertion. For example, none of the cited art discloses that CO is used to improve an etching profile while etching a dielectric layer. Therefore, Applicants respectfully request citation of a reference supporting this assertion if the assertion is maintained.

For at least the reasons stated above, none of the cited art teaches or suggests the limitations of claims 1, 17, and 21. Therefore, claims 1, 17, and 21, and claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of the § 103(a) rejections of claims 1-5 and 7-27 is respectfully requested.

CONCLUSION

In this response, claims 1, 5, and 15 have been amended. Rejections of claims 1-5 and 7-27 have been addressed. Therefore, this response constitutes a complete response to all of the issues raised in the Office Action mailed April 26, 2002. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-5 and 7-27 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

The Commissioner is authorized to charge any required fees or credit any overpayment to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-04100.

ATTACHMENT A
"Marked-Up" Amendments

IN THE CLAIMS:

Please amend claims 1, 5, and 15 as follows:

1. (Twice Amended) A method for forming a semiconductor device, comprising:

etching a first portion of a dielectric layer formed on a semiconductor topography with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen and comprises C_4F_8; and

etching a second portion of the dielectric layer with a second etch chemistry different from the first etch chemistry, wherein the first and second etch chemistries are selective to silicon nitride.

5. (Twice Amended) The method of claim 1, wherein the semiconductor topography comprises a gate structure formed on a semiconductor layer, and wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of [a] the gate structure [formed adjacent to the second portion].

15. (Amended) The method of claim 1, wherein the semiconductor topography comprises a gate structure formed on a semiconductor layer, wherein the semiconductor layer comprises isolation regions, and wherein the dielectric layer is in contact with a sidewall spacer of [a] the gate structure and [a] the semiconductor layer [comprising isolation regions].